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09/932,891	08/20/2001	Jens Sauerbrey	L&L-10050	6815

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EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 04/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,891	SAUERBREY ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment dated March 21, 2005.

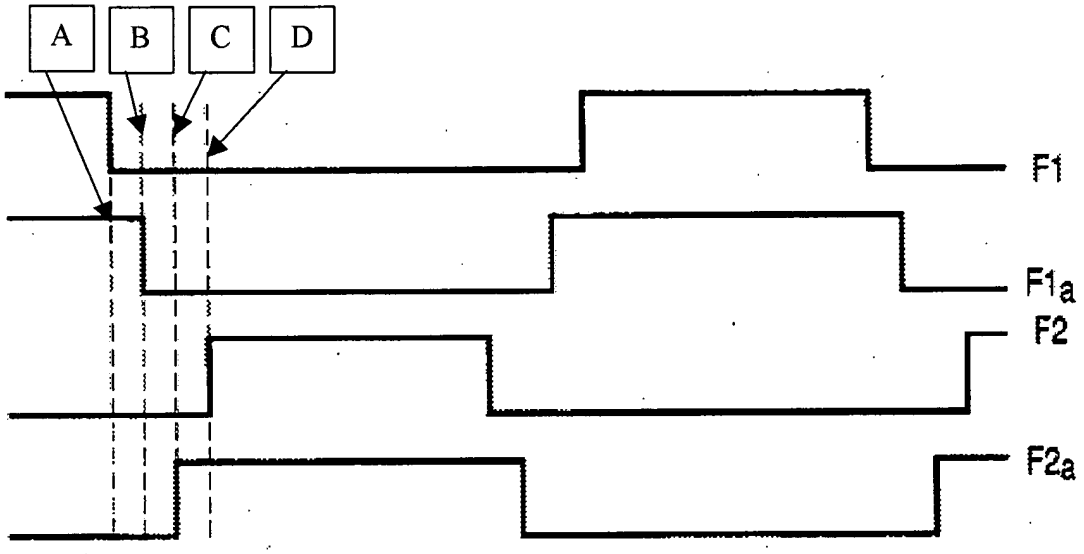
2. Claims 1-5 and 7-31 are presented for examination. Applicant has canceled claim 6.

3. The following are fact findings supporting the rejection of claims 1 and 15-17:

Findings

4. Baschirotto et al. and Fletcher were cited as prior art in previous Office Action.

5. Baschirotto et al., U.S. Patent 5745002, hereinafter Baschirotto, discloses:



5.1. A circuit configuration in switched op-amp technology [fig.9; col.4, ll.21-23].

5.2. The circuit configuration comprising at least one switchable operational amplifier [A2] having an input [S4] and an output [VO] [fig.4] and transistors having a switching speed [fig.10; inherently, transistors have associated switching speed dependent upon their respected dimensions].

5.3. The circuit configuration comprising at least one sampling capacitor [switched or sampling capacitance C1] connected to said input.

5.4. The circuit configuration comprising at least one integrating capacitor [feedback capacitance C2] connected to said input and to said output.

5.5. The circuit configuration comprising a clock generator [inherently, there is a clock generator, *in the broadest interpretation*, to produce the signals] producing at least two non-overlapping switching-clock signals [fig.5, F1 and F2].

5.6. Each clock signal having switching-clock phases including an on-phase and an off-phase [col.8, ll.1-8, l.60 – col.9, l.14].

5.7. Said at least two non-overlapping switching-clock signals including a first switching-clock signal [F1] and a second switching-clock signal [F2].

5.8. Said clock generator controlling charging of said sampling capacitor with said first switching-clock signal [col.9, ll.7-10] and switching said operational amplifier on and off with said second switching-clock signal [col.9, ll.10-14; controls on/off of output].

5.9. The circuit configuration comprising a phase-variance device [fig.5; inherently, there is a phase-variance device, *in the broadest interpretation*, to output the different phases] varying said switching-clock phases in which said first and second switching-clock signals are in said off-phase [col.8, ll.1-5; suitably delaying or varying the phases].

5.10. A circuit configuration [fig.8] in fully differential circuit technology [col.4, ll.1-15; the signal lines and voltage settings of the circuit configuration of fig.4 may also be set accordingly to derive the fully differential configuration].

5.11. A method for clocking successive operation amplifier stages [fig.9; op-amp 1, 2, and 3 form successive stages] constructed in switched op-amp technology [col.4, ll.21-23].

5.12. The method comprising generating at least two non-overlapping switching-clock signals [F1a and F2a] [fig.5; col.8, ll.1-8, l.60 – col.9, l.14].

5.13. The method comprising switching a first operational amplifier [A1] on and off with a first signal [F1a] of the two switching-clock signals [col.9, ll.40-44].

5.14. The method comprising switching a second operational amplifier [A2] on and off with a second signal [F2a] of the switching-clock signals [col.9, ll.58-62].

5.15. The method comprising varying switching-clock phases of the first [F1a] and second [F2a] signals in which the operational amplifiers are switched off [col.8, ll.1-5; suitably delaying or varying the phases].

5.16. The method comprising providing a variable delay between the switching-clock phases of the first [F1a] and second signals [F2a] during which the operational amplifiers are switched off [fig.5; col.7, l.62 – col.8, l.5; suitably delaying or varying the phases].

5.17. The phase-variance device being configured for varying a duration of the switching-clock phases in which the first and second switching-clock signals are in the off-phase dependent upon the switching speed of the transistors [col.7, l.6 – col.8, l.5; anticipating the switching function to control the negative spikes suggests utilization of knowledge of switching speed of the transistors in order to derive appropriate timing].

6. Fletcher, U.S. Patent 6392466, discloses:

6.1. A circuit configuration [cache 700; fig.3] in switched amplifier [sense amplifier 620] technology [fig.5; col.3, l.46 – col.4, l.2].

6.2. The circuit configuration comprising a clock generator [703].

6.3. The circuit configuration comprising a phase-variance device [controllable pulse clock delay block 790] varying said switching-clock phases in which the first and second switching-clock signals are in off-phase [fig.6; col.21, l.19 – col.22, l.5; control signals enable phase two to be off-phase relative to phase one].

6.4. Said phase-variance device connected to said clock generator [fig.3].

6.5. The advantage of utilizing phase variance in circuits is reduction in power consumption [col.8, ll.41-65; pulse clock delay arrangement varies phase and thus, produces a pulse with suitable width to save processing time which saves power].

7. Saito et al., U.S. Patent 5723998, hereinafter Saito, discloses:

7.1. A circuit configuration, comprising a detector [operating speed measurement 121] for detecting the switching speed of the transistors, the detector being connected to an operational amplifier [comparator 139] [col.5, l.35 – col.6, l.39].

7.2. The advantage of utilizing a transistor speed detector is optimization of processing according to operating condition [col.1, ll.49-67].

8. Varadarajan, U.S. Patent 4551638, discloses:

8.1. A circuit configuration comprising a device [ECL gate] for enlarging a duration [from activation of driving signal which switches the transistor to onset of delay] when a switching speed is high and reducing the duration when the switching speed is low [switching speed is inversely related to delay] [col.3, ll.42-57].

8.2. The advantage of enlarging a duration when a switching speed is high and reducing the duration when the switching speed is low is to reduce power consumption without adversely affecting performance.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Re Claims 17-21 and 24

10. Claims 17-21 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Baschirotto.

11. In re claim 17, Bashirotto discloses each and every claimed limitation as set forth in findings 5.11-5.16.

12. As to claim 18, Baschirotto discloses the method comprising:

12.1. Varying each of the switching-clock phases in which the operational amplifiers are switched off [finding 5.15; in fig.5 reproduced above, both switching-clock phases of F1a and F2a are varied resulting in both clock signals being in the off-phase in the interval between B and C].

13. As to claim 19, Baschirotto discloses the method comprising:

13.1. Varying each second one of the switching-clock phases in which the operational amplifiers are switched off [in fig.5 reproduced above, phase of F2 is varied resulting in F1 and F2 being in off-phase in the interval between A and D].

14. As to claim 20, Baschirotto discloses the method comprising:

14.1. Varying a duration of the switching-clock phases in which the operational amplifiers are switched off dependent on a transient response of the operational amplifiers [col.7, l.62 – col.8, l.5; anticipating the switching function to control the negative spikes

suggests utilization of knowledge of transient response in order to derive appropriate timing].

15. As to claim 21, Baschirotto discloses the method comprising:

15.1. Varying a duration of the switching-clock phases in which the operational amplifiers are switched off dependent on a switching speed of transistors of the operational amplifiers [fig.10; col.7, l.6 – col.8, l.5; anticipating the switching function to control the negative spikes suggests utilization of knowledge of switching speed of the transistors in order to derive appropriate timing].

16. As to claim 24, Baschirotto discloses the method comprising:

16.1. Adjusting a duration of the switching-clock phases in which the operational amplifiers are switched off in a number of predetermined steps [col.7, l.62 – col.8, l.5; anticipating the switching function to control the negative spikes suggests a method comprising a number of predetermined steps such as taking in the current relevant values of clock, voltage, etc., comparing the values to some predetermined value, and then act accordingly in order to derive appropriate timing].

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Re Claims 1-5, 7, 9-12, and 15-16

18. Claims 1-5, 7, 9-12, 15-16, and 28-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baschirotto in view of Saito, Varadarajan and Fletcher.

19. In re claim 1, Baschirotto discloses each and every limitation of the claim [findings 5.1-5.9, 5.17]. Baschirotto did not discuss a detector for detecting the switching speed of the transistors and did not discuss the details of the phase-variance device. Saito discloses a circuit configuration, comprising a detector for detecting the switching speed of the transistors, the detector being connected to an operational amplifier [finding 7.1] in order to optimize processing [finding 7.2]. It would have been obvious to one of ordinary skill in the art, having the teachings of Baschirotto and Saito before him at the time the invention was made, to use the detector taught by Saito for the circuit configuration disclosed by Baschirotto as the detector taught by Saito is suitable for use in the circuit configuration of Baschirotto. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to optimize processing. Varadarajan discloses a circuit configuration comprising a device for enlarging a duration when a switching speed is high and reducing the duration when the switching speed is low [finding 8.1] in order to reduce power consumption without adversely affecting performance [finding 8.2]. It would have been obvious to one of ordinary skill in the art, having the teachings of Baschirotto and Varadarajan before him at the time the invention was made, to use the teachings of Varadarajan for the circuit configuration disclosed by Baschirotto as the teachings of Varadarajan is suitable for use with the phase-variance device of Baschirotto. One of ordinary skill in the art would have been motivated to make such a combination as it provides

a way to reduce power consumption without adversely affecting performance. Fletcher teaches a circuit configuration in switched amplifier, comprising a clock generator connected to a phase-variance device for varying the switching-clock phases in which the first and second switching-clock signals are in off-phase [findings 6.1-6.4], in order to reduce power consumption [finding 6.5]. It would have been obvious to one of ordinary skill in the art, having the teachings of Baschirotto and Fletcher before him at the time the invention was made, to use the phase-variance device taught by Fletcher for the circuit configuration disclosed by Baschirotto as the phase-variance device taught by Fletcher is suitable for use as the phase-variance device of Baschirotto. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to reduce power consumption.

20. As to claim 2, Baschirotto discloses the circuit configuration wherein:

20.1. The phase-variance device is configured to vary each of said switching-clock phases in which the first and second switching-clock signals are in the off-phase [finding 5.9; in fig.5 reproduced above, both switching-clock phases of F1a and F2a are varied resulting in both clock signals being in the off-phase in the interval between B and C].

21. As to claim 3, Baschirotto discloses the circuit configuration wherein:

21.1. The phase-variance device is configured to vary each second one of the switching-clock phases in which the first and second switching-clock signals are in the off-phase [finding 5.9; in fig.5 reproduced above, phase of F2 is varied resulting in F1 and F2 being in off-phase in the interval between A and D].

22. As to claim 4,

22.1. The Examiner hereby takes Official Notice that operational amplifiers have an associated transient response [operational amplifiers are signal control devices that operate on electrical power and thus, have a time duration for output power levels to stabilize].

22.2. Baschirotto discloses the phase-variance device is configured to vary a duration of the switching-clock phases in which the first and second switching-clock signals are in the off-phase dependent upon the transient response of the operational amplifier [col.7, l.62 – col.8, l.5; anticipating the switching function to control the negative spikes suggests utilization of knowledge of transient response in order to derive appropriate timing].

23. As to claim 5, Baschirotto discloses the circuit configuration wherein:

23.1. The operational amplifier has transistors [fig.10] having a switching speed [inherently, transistors have associated switching speeds dependent upon their respected dimensions].

23.2. The phase-variance device is configured to vary a duration of the switching-clock phases in which the first and second switching-clock signals are in the off-phase dependent upon said switching speed of the transistors [col.7, l.6 – col.8, l.5; anticipating the switching function to control the negative spikes suggests utilization of knowledge of switching speed of the transistors in order to derive appropriate timing].

24. As to claim 7,

24.1. Baschirotto discloses the circuit configuration wherein the transistors include at least one of n-channel FETs and p-channel FETs [fig.10] and the transistors each have a

respective switching speed [inherently, each transistor will have a switching speed in the broadest interpretation].

24.2. Saito discloses the detector detects the switching speed of the transistors [col.5, ll.35-57; detector detects switching speed of at least one of the kind of transistors].

25. As to claim 9, Saito discloses the circuit configuration wherein the detector generates detector pulses having a duration characterizing the switching speed of the transistors [col.5, l.35 – col.6, l.38; variable number of pulses of variable duration based on the switching speed of the transistors occupy a predetermined time period to constitute the count value].

26. As to claim 10, Baschirotto and Saito disclose the circuit configuration wherein the phase-variance device is configured to adjust a duration the switching-clock phases in which the first and second switching-clock signals are in the off-phase dependent upon a duration of the detector pulses [finding 5.9 and discussion above in reference to claim 9; detector pulse with variable duration of Saito combined with phase variance device of Baschirotto results in adjusting the duration of switching-clock phases in the broadest interpretation].

27. As to claim 11, Baschirotto discloses the circuit configuration wherein:

27.1. The phase-variance device is configured to adjust a duration of the switching-clock phases in which the first and second switching-clock signals are in the off-phase in a given number of predetermined steps [col.7, l.62 – col.8, l.5; anticipating the switching function to control the negative spikes suggests a method comprising a number of predetermined steps such as taking in the current relevant values of clock, voltage, etc., comparing the values to some predetermined value, and then act accordingly in order to derive appropriate timing].

28. As to claim 12, Fletcher discloses the circuit configuration wherein:

28.1. The clock generator and the phase-variance device are embodied as a programmable clock generator [col.22, ll.6-35; clock generator and phase-variance device may be integrated as a programmable clock generator for each logical unit].

29. As to claim 15, see finding 5.10 and discussion above in reference to claim 1.

30. As to claim 16, see discussion above in reference to claim 1 and the following:

30.1. In regards to "a means for generating at least two non-overlapping switching-clock signals each having an on-phase and an off-phase", see finding 5.5 where the clock generator represents the means.

30.2. In regards to "a means for varying switching-clock phases in which said first and second switching-clock signals are in said off-phase", see finding 5.9 where the phase-variance device represents the means.

31. As to claim 28, see discussion above in reference to claims 1 and 17.

32. As to claim 29-31, see discussion above in reference to claims 7 and 15-17.

Re Claim 8

33. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saito, Baschirotto and Fletcher as applied to claim 1 above, and further in view of Chiang, U.S. Patent 5097208.

34. Saito, Baschirotto and Fletcher disclose each and every limitation of the claim as discussed above in reference to claim 1. In particular, Saito discloses the circuit configuration including an inverter chain [fig.6; inverters 31-35]. Saito, Baschirotto and Fletcher did not further discuss the details of the detector.

35. Chiang discloses a detector [testing apparatus 10] [col.1, ll.8-13; delays are related to speed] having an XOR gate [14] with XOR inputs, one of the XOR inputs receiving an undelayed edge signal [B], and another of the XOR inputs receiving the edge signal delayed through the inverter chain [C] [fig.1; col.3, ll.15-34].

36. It would have been obvious to one of ordinary skill in the art, having the teachings of Chiang, Saito, Baschirotto and Fletcher before him at the time the invention was made, to use the detector taught by Chiang for the circuit configuration disclosed by Saito, Baschirotto and Fletcher as the detector taught by Chiang is suitable for use in the circuit configuration of Saito, Baschirotto and Fletcher. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to determine the speed of an integrated circuit [col.1, ll.8-37; delays are related to speed].

Re Claims 13-14

37. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito, Baschirotto and Fletcher as applied to claim 1 above, and further in view of Larson, U.S. Patent 4951303.

38. In re claim 13, Baschirotto and Fletcher disclose each and every limitation of the claim, as discussed above in reference to claim 1. Baschirotto and Fletcher did not disclose the embodiment details of the clock generator and the phase-variance device.

39. Larson discloses a circuit configuration comprising a clock generator [square wave generator circuit 20] and a phase variance device [ring oscillator 40] embodied as:

39.1. An external squarewave generator [25] producing a squarewave signal [col.2, ll.50-51].

39.2. A divider circuit [primarily ring oscillator 40] connected to the squarewave generator, the divider circuit generating the at least two switching-clock signals from the squarewave signal [col.2, l.49 – col.3, l.39; lines 22 and 24 produce the two different phase signals with the output being controlled by terminal 56].

40. It would have been obvious to one of ordinary skill in the art, having the teachings of Larson, Saito, Baschirotto and Fletcher before him at the time the invention was made, to use the clock generator and phase-variance device taught by Larson for the circuit configuration disclosed by Saito, Baschirotto and Fletcher as the clock generator and phase-variance device taught by Larson is suitable for use in the circuit configuration of Saito, Baschirotto and Fletcher. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to reduce power consumption [finding 6.5].

41. As to claim 14, Baschirotto discloses the circuit configuration wherein:

41.1. The squarewave signal has a duty ratio [fig.5; inherently, squarewaves generated have an associated duty ratio with the ideal being 1:1].

41.2. Adjustment of the duty ratio varies the switching-clock phases in which the first and second switching-clock signals are in the off-phase [fig.5 and finding 5.9; the duty ratio of F2 is not an ideal 1:1 and has been adjusted through phase-variance device to result in the off-phase interval as discussed above in reference to claim 3].

Re Claims 22-23

42. Claims 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baschirotto, as applied to claims 17 and 21 above, and further in view of Saito.

43. Baschirotto discloses each and every limitation of the claim as discussed above in reference to claims 17 and 21 above. Baschirotto did not discuss a detector for detecting the switching speed of the transistors. Saito discloses a circuit configuration, comprising a detector for detecting the switching speed of the transistors [finding 7.1] in order to optimize processing [finding 7.2]. It would have been obvious to one of ordinary skill in the art, having the teachings of Baschirotto and Saito before him at the time the invention was made, to use the detector taught by Saito for the circuit configuration disclosed by Baschirotto as the detector taught by Saito is suitable for use in the circuit configuration of Baschirotto. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to optimize processing.

Re Claims 25-27

44. Claims 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baschirotto as applied to claim 17 above, and further in view of Larson.

45. In re claim 25, Baschirotto discloses each and every limitation of the claim, as discussed above in reference to claim 17. Baschirotto did not disclose the details of a specific clock generator for generating the clock signals.

46. Larson discloses a method for generating clock signals [frequency] [col.1, ll.8-10] with a programmable clock generator [frequency divider 10] [col.2, l.67 – col.3, ll.39; clock generator is programmed through terminal 56 to output appropriate clock signals].

47. It would have been obvious to one of ordinary skill in the art, having the teachings of Larson and Baschirotto before him at the time the invention was made, to use the programmable clock generator taught by Larson in the method disclosed by Baschirotto as the clock

generator taught by Larson is suitable for use in the method of Baschirotto to produce the at least two non-overlapping switching-clock signals. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to produce the switching-clock signals.

48. As to claim 26, see discussion above in reference to claim 25. Larson discloses a method for generating clock signals with an external squarewave generator [25] and a divider circuit [primarily ring oscillator 40].

49. As to claim 27, Baschirotto discloses the method comprising:

49.1. Varying the switching-clock phases in which the operational amplifiers are switched off by adjusting a duty ratio of a squarewave signal from the squarewave generator [fig.5 and finding 5.9; the duty ratio of F2 is not an ideal 1:1 and has been adjusted to result in the off-phase interval as discussed above in reference to claim 19].

Response to Arguments

50. All rejections of claim limitations as filed prior to Amendment dated March 21, 2005 not argued in entirety or substantively in response filed as said Amendment have been conceded by Applicant and the rejections are maintained from henceforth.

51. Applicant's arguments filed March 21, 2005 have been fully considered but they are not persuasive.

52. Applicant alleges in various forms that "Baschirotto discloses ... providing for suitably delayed clock phase signals, the delay being sufficiently large to suppress unwanted switching spikes when turning on operational amplifiers in a switched op-amp configuration... does not suggest providing a variable delay within the circuit as recited in

the instant claims... simply provides for a fixed, non-variable delay which is in any case ... sufficiently large to suppress the unwanted switching spikes". Firstly, Examiner respectfully submits that Applicant's allegation is a mere conclusion without indicating specifically where Baschirotto actually stipulates that the delay must be sufficiently large in order to suppress unwanted switching spikes. Secondly, Examiner notes with appreciation that Applicant concedes Baschirotto does indeed provide for suitably delayed clock phase signals by citing col.7, l.62 – col.8, l.5. Alas, the citation points out a serious flaw in Applicant's own reasoning and strengthens Examiner's position instead. According to the citation, Baschirotto reduces "the amplitude of the negative switching spikes consists in anticipating the turning on of ... A1 ***and*** ... A2". If Baschirotto were to disclose a fixed delay system, there would be no reason to anticipate the turning on of ***both*** A1 and A2 [i.e., only the input A1 would have to be anticipated in the hypothetical case of a fixed delay system]. Instead, Baschirotto specifically discloses the anticipation of ***both*** A1 and A2 because there is variation [i.e., variable delay] between A1 and A2.

53. Applicant alleges that Baschirotto's "text does not disclose a delay between the signals F1a and F2a", but concedes that "the only relevant disclosure [of the delay]... is shown in figure 5". Examiner is perplexed as to why Applicant would insist Baschirotto be required to document in text what is illustrated clearly in a figure. Examiner reminds Applicant that figures are part of a patent disclosure that can aid in comprehension.

54. Applicant alleges that Baschirotto "does not disclose anything ... about the size or the necessity of the delay between signals F1a and F2a". Applicant's allegation appears to be arbitrary for the sake of argument without any indication of relevance, resulting in a direct

contradiction to Applicant's earlier allegation that Baschirotto discloses the delay "being sufficiently large to suppress the unwanted switching spikes". Examiner invites Applicant to read/review 37 CFR 1.111 in order to comply with the expected constructs of an argument for a reply to an Office Action.

55. Applicant alleges that claim 1 "is not obvious in view of Bashirotto, Saito, and Fletcher", and then proceeded to list the references' individual deficient teachings. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

56. Applicant alleges that "Fletcher's teaching to generate a delayed output clock signal based on an input clock signal neither relates to the common off-phase of two clock signals nor to non-overlapping signals or switched op-amp technology in general as set forth in the claims of the instant application." In response to applicant's argument that Fletcher is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Fletcher deals with variable delay signals and the problems associated with control of the variable delay signals.

57. Applicant alleges that Saito "does not disclose distinguishing between n-and p-channel transistors when detecting the switching speed of transistors ... Saito's approach ... is to ...

whereby a single value is detected which depends on the switching speed of ***both*** n- and p-channel transistors". Firstly, Examiner again respectfully submits that Applicant's allegation is a mere conclusion without indicating specifically where Saito actually stipulates that the switching speed must be of ***both*** n- and p-channel transistors. Examiner invites Applicant to read Saito thoroughly and note that Saito teaches a ***general*** detector that can detect the switching speed of any type of transistor. Secondly, Examiner again reminds Applicant that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. In the instant case, Examiner notes that Applicant conveniently disregarded Baschirotto's teaching of the circuit configuration wherein the transistors include at least one of n-channel FETs and p-channel FETs and the transistors each have a respective switching speed. Baschirotto's particular teaching combined with Saito's ***general*** detector of transistor switching speed in order to optimize processing would have been obvious to one with ordinary skill in the art.

58. Applicant alleges that the references do not show a circuit "including an inverter chain, said detector having one of: an XOR gate with XOR inputs, one of said XOR inputs receiving an undelayed edge signal, and another of said XOR inputs receiving an edge signal delayed through said inverter chain; and an XNOR gate with XNOR inputs, one of said XNOR inputs receiving an undelayed edge signal and another of said XNOR inputs receiving an edge signal delayed through said inverter chain". Applicant did not provide any support for the allegation. Examiner again invites Applicant to read/review 37 CFR 1.111 in order to comply with the expected constructs of an argument for a reply to an Office Action.

59. All other claims were not argued separately.

Conclusion

60. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

61. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

62. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

63. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

64. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information

about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Tse Chen
April 15, 2005